UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,137	09/30/2003	Frank E. LeClerg	884.A46US1	6409

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EXAMINER
KERVEROS, JAMES C

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
04/23/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _29 February 2008_.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-25_ is/are pending in the application.
    4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) _1-25_ is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☒ The drawing(s) filed on _09/30/2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.
    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
    a)☐ All b)☐ Some * c)☐ None of:
      1.☐ Certified copies of the priority documents have been received.
      2.☐ Certified copies of the priority documents have been received in Application No. _____.
      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .
5)☐ Notice of Informal Patent Application
6)☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/31/2008 has been entered.

This is a Non-Final Office Action in response to the Amendment filed 2/29/2008. Claims 1-25 are presently under examination and pending.

Response to Arguments

Applicant's arguments filed on 2/29/2008, with respect to the final rejection of claims 1-25 under 35 USC 102(e) as being anticipated by Moyes et al. (US 7,065,688), have been fully considered and are persuasive. Therefore, the final rejection has been withdrawn. However, upon a new ground of rejection, Grimes discloses a method for initializing a system memory 40 and a memory controller (36, 37) for accessing data from the memory, Figs. 2, 3, 8, as set forth in the present Office Action.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Grimes (US Patent No. 5,684,979), issued: November 4, 1997.

Regarding independent Claims 1, 5, 8, 12, 16, 21, Grimes discloses a method for initializing a system memory 40, which is a page mode memory and a memory controller (36, 37) for accessing data from the memory, Figs. 2, 3, 8, comprising:

A first memory access procedure generated in the CPU 30 (Fig . 3), which uses a plurality of its general purpose registers R0-R9, its adder circuit 72, and an adder register 73, together with the presence register 70, the ID register 71, and the memory address programming registers PR0-PR7 to initialize the memory 40 and memory controller 36, described below.

Performing the first memory access procedure in response to receiving a first memory access procedure command (RAS/CAS/WE) over a command bus (Memory Bus) from the memory controller (36).

The first memory access procedure causes a memory module (51-0 to 51-7), Fig. 3 single in-line memory modules (SIMM), which are installed in sockets 61-0 to 61-7 of memory 40 to perform multiple accesses of first memory locations associated with the memory module.

The first memory access procedure includes a memory initialization procedure (step 100) and a memory test procedure (step 100), as shown in the flow chart of Fig. 8,

which describes the initialization process performed by the CPU 30 in accordance with memory initialization firmware stored in the ROM 42 and transferred to the L1 cache in CPU 30 for execution.

Regarding Claims 2-4, 6, 7, 9-11, 13-15, 17-20, 22-25, Grimes discloses the memory controller (36) connecting the processor 30 and the memory system 40 for controlling the accessing of the memory system, using memory module start addresses, during the execution of program instructions by the processor, the memory modules being available in differing memory sizes, a method for initializing the memory system and the memory controller through a process of configuration, testing and reconfiguration, comprising the steps of the flow chart of Fig. 8.

In Fig. 8, the memory initialization is started (step 100) by determining the configuration of the memory 40 (step 101). The memory controller 36 is programmed for the attached configuration (step 102). Memory is tested in step 103 and if one or more errors were detected (step 104), the faulty SIMMs are logically removed from the configuration (step 105) and the Memory Controller 36 is reprogrammed (step 106) for the new configuration. After reprogramming in step 106, or in the event that no error was detected in step 104, the program returns to the main firmware routines, step 107.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to JAMES C. KERVEROS whose telephone number is

(571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Jacques H. Louis-Jacques can be reached on (571) 272-4150. The fax

phone number for the organization where this application or proceeding is assigned is

571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/JAMES C KERVEROS/
Primary Examiner, Art Unit 2117

Date: 23 April 2008
Office Action: Non-Final Rejection

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